

SPACE-BASED DATA CENTERS ROADMAP: THE CASE FOR CAUTION

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CHAPTER 1.4:

Radiation Hardening

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WORKING PAPER

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MAIN MESSAGES

- Radiation levels are higher in space than on Earth. Satellites in low Earth orbit (LEO) are exposed to ionizing radiation from multiple sources that can interfere with, or even destroy, artificial intelligence (AI) chips. The exact amount of exposure depends on the altitude and inclination of the satellite's orbit.
- There are multiple methods to reduce this exposure, including shielding with aluminum or other materials, modifying semiconductor manufacturing processes, or adding redundancy and additional tolerances through software. However, these all lead to additional costs and reduced performance.

Data centers in low Earth orbit (LEO) are exposed to more and different ionizing radiation than on Earth. This radiation can damage or destroy electronics, such as processors and memory. These issues can be partly addressed through engineering and design, but measures for addressing them typically add mass and negatively impact performance. Although methods for protecting conventional computing equipment from radiation in space are well known, the space industry has little experience in protecting AI-grade chips from radiation in LEO.

A. Radiation in Space

Space is filled with radiation from multiple sources. Much of this radiation never reaches the surface of the Earth because the planet's magnetic field and atmosphere deflect or absorb it (see Figure 1). However, satellites in LEO are exposed to three main sources of radiation that do not significantly impact Earth[1]:

- Earth's radiation belts (ERBs): High-energy electrons and ions that form two belts in the Earth's inner magnetosphere (the Van Allen belts, see Figure 2). The energy these particles carry typically ranges from roughly 10 keV to 100s of MeV.
- Galactic cosmic rays (GCRs): Charged particles, most of which are protons, from outside the solar system and traveling at high speed (see Figure 3). The energy these rays carry typically ranges from roughly 100 MeV to 1 GeV.
- Solar particle events (SPEs): High-energy particles (primarily protons) emitted from the Sun during solar flares and coronal mass ejections (CMEs) (see Figure 4). The energy these particles carry typically ranges from roughly 10 MeV to 100s of MeV.

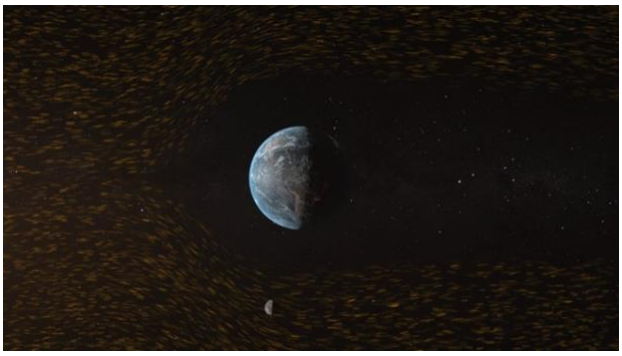


Figure 1. *Earth's magnetic field and atmosphere*

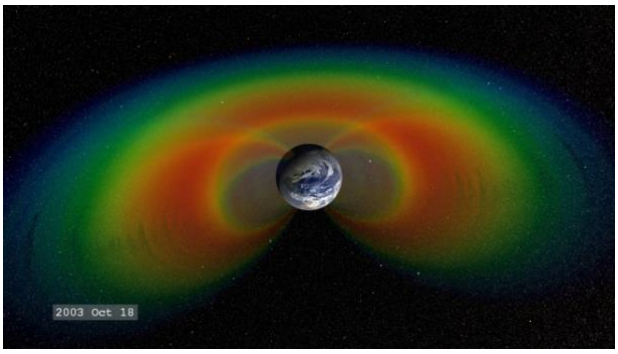


Figure 2. *The Van Allen belts*

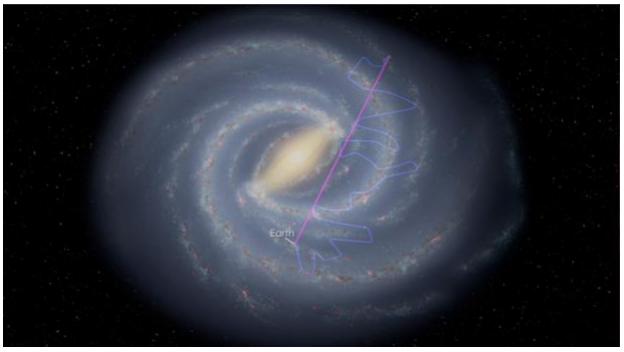


Figure 3. *A galactic cosmic ray's path from outer space to low Earth orbit*

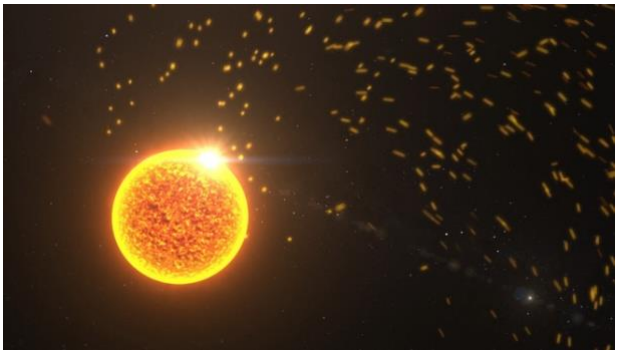


Figure 4. *Solar particle events: a solar flare and coronal mass ejection*

Source: NASA's Goddard Space Flight Center

Satellites in LEO are exposed to varying amounts of radiation depending on altitude and orbital inclination. For low-altitude LEO, the Earth's magnetic field shields satellites relatively well from GCR and SPE radiation.[1] As altitude increases, this protection decreases. Satellites in LEO at low orbital inclination (orbits that stay close to the equator) receive much less GCR and SPE radiation compared to high orbital inclination because Earth's magnetic field is strongest near the equator and more effectively deflects these particles. Low-inclination satellites also receive less ERB radiation than higher inclination satellites because the Van Allen belts are typically higher near the equator.[2] The inner Van Allen belt dips anomalously low over a region of the South Atlantic Ocean known as the South Atlantic Anomaly (SAA).[3] Earth's magnetic field is significantly weaker over the SAA (see Figure 5). Satellites in moderate- to high-inclination LEO, including Sun-synchronous orbits (SSOs), can pass over the SAA, exposing them to ionizing radiation doses up to two orders of magnitude higher than at other latitudes in the same orbit.[4]

For satellites in LEO with 1 mm of aluminum radiation shielding, the annual radiation dosage typically ranges from 100 to 10,000 rad (a unit equivalent to 1 centiGray (cGy)). The higher dosages occur at higher altitudes and higher inclinations. In some high-altitude, high-inclination LEOs, annual dosages

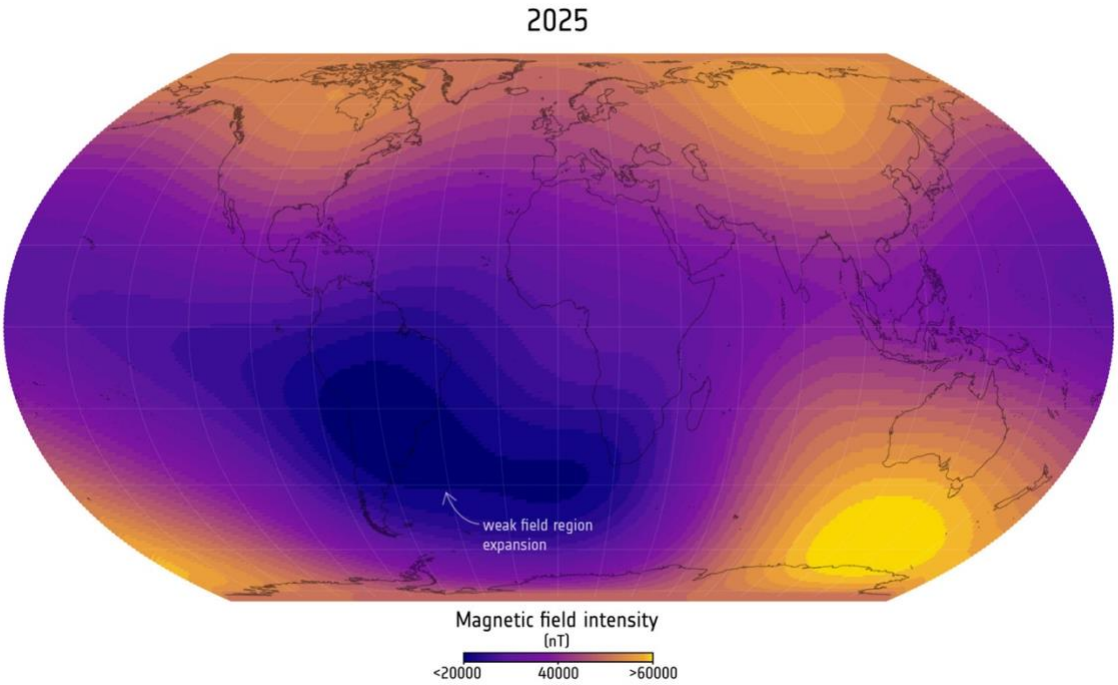


Figure 5. *The South Atlantic Anomaly in 2025. Source: ©ESA, Finlay, C.C. et al., 2025. Open Access, CC BY 4.0*

with only this thin 1 mm aluminum shielding can reach values even higher than 10,000 rad. Thicker shielding reduces this total dosage by blocking radiation, but it leads to additional weight and cost.

B. Impact of Radiation on AI Chips

The impact of radiation on AI chips can be categorized as follows:

- Single event effects (SEEs): Effects caused by a single energetic radiation particle strike. SEEs range from transient, recoverable effects (e.g., bit flips and logic glitches) to permanent, destructive damage (e.g., a latch-up) that can destroy a device.
- Total ionizing dose (TID): Cumulative degradation of AI chips due to radiation exposure over time.

AI processors and memory chips consist of billions of silicon transistors. Circuits built from these transistors store binary data and execute instructions by turning tiny semiconductor switches on and off. A thin oxide layer known as the gate oxide insulates each transistor's switching signal. When ionizing radiation strikes an oxide layer, positive charge can accumulate and become trapped in the silicon-oxide layer.[5]

SEEs can arise when the charge deposited by a single high-energy particle striking a transistor degrades it immediately. SEEs can also occur in indirect cases where a particle collides with a silicon nucleus and produces high-energy secondary fragments. In some cases, these strikes lead to a bit flip, in which a bit switches from a 0 to a 1 or vice versa, corrupting a piece of data. This can occur in the AI chip's stored data or in its control logic, causing it to crash and require a reset. Most severely,

if the charge from a single strike exceeds a critical threshold, it can trigger a short circuit inside a chip, known as a single-event latch-up, that can cause permanent damage if it is not detected and shut down quickly.



Figure 6. *Intel's Myriad 2. Source: CERN/Maximilien Brice*

TID measures how trapped charge accumulates over time in the oxide. As charge builds up, it gradually shifts a transistor's threshold voltage (i.e., the voltage needed to turn it on or off). Enough threshold voltage shift can prevent a transistor from correctly switching and/or can result in current leakage even when it should be off, degrading the chip's performance and leading to eventual failure. For modern AI chips, the isolation oxide between transistors is often a more significant site for radiation-induced charge trapping and leakage than the gate oxide. This is because modern fabrication processes have reduced the gate oxide thickness dramatically. Simultaneously, as these feature sizes continue to shrink, they hold less electric charge and become even more sensitive to SEEs. A single-particle strike can also flip multiple adjacent memory cells because of this reduced size and close packing.

C. Strategies for Radiation Hardening

Multiple techniques can be used to make AI chips resistant to damage from radiation in LEO ("radiation-hardening"). However, because these all have costs and performance drawbacks, devices are first subjected to radiation testing to determine which forms of "hardening" are required.

Notably, some commercial off-the-shelf (COTS) computer hardware is relatively resistant to radiation without any modifications. For example, the European Space Agency's (ESA's) 2018 test on the Intel Myriad 2 (Figure 6) demonstrated the chip had enough radiation tolerance for space travel without hardening.[6] However, this chip is not suited for the type of AI applications that would be carried out on an SBDC.

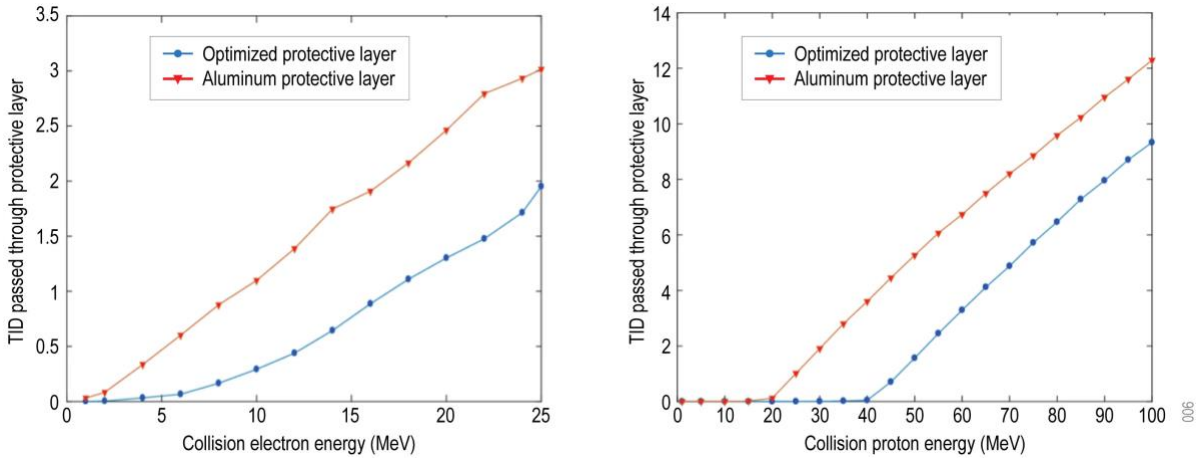
A more relevant example is from Google, which demonstrated the first radiation test of a high-performance processor—their Trillium tensor processing unit (TPU)—in 2025 using a proton beam to simulate the radiation dose of a five-year LEO mission. While the TPU's high-bandwidth memory (HBM) showed some performance issues after being irradiated, the core logic and compute functions experienced no hard failures up to a very high radiation dose.[7] SEEs caused occasional "silent" data corruption—faults that altered data or a computed result without being detected by the system—at a rate of 1 inference failure per 3 million.[7] This radiation test simulated 10 mm of aluminum radiation shielding on the chip, reducing the TID significantly. This type of TPU is directly used in AI applications, and these results suggest that AI chips may require somewhat less radiation hardening than expected, although far more testing is required to validate this.

Primary radiation hardening methods include the following:

i. Structural hardening and shielding

Ionizing radiation can be partly blocked by adding layers of shielding material around electronics. Many satellites use aluminum for overall structural support and take advantage of its moderate radiation shielding ability to offer partial protection. Better shielding materials can be used in addition to aluminum or on their own when structural support is not required. For example, multilayer shields of lithium hydride (an effective material because of its capacity to store hydrogen) and polyethylene (used for its tensile strength) have shown promise[8] for blocking GCR. To shield against trapped electrons and protons in LEO, triple-layering dense metals, such as gold, lead, tungsten and tantalum, combined with aluminum can reduce TID by up to 70% against electron sources and 50% against proton sources compared to simple aluminum (see Figures 7 and 8).[9]

While this shielding can reduce radiation damage to AI chips and prolong their life, the added mass also increases the overall cost of a spacecraft. Additionally, these specific, multi-layer designs remain research prototypes that have not yet been flown operationally. Process innovations and flight validation will be required to make lighter layered shield designs for AI chips economically viable at scale.



Figures 7, 8. *Each blue curve's "optimized protective layer": gold-tungsten-aluminum for electron environment and tungsten-lead-tantalum for proton environment. Source: Daneshvar, H., Milan, K. G., Sadr, A., et al., 2021.9 Open Access*

ii. Doping transistors

Radiation-hardening-by-design (RHBD) methods modify a transistor's manufacturing process before radiation exposure. These include building enclosed layout transistors by reshaping transistor gates into closed rings to prevent charge leakage, placing "guard rings" around transistors to protect against SEEs,[10] and modifying and controlling chip silicon-on-oxide layer growth. A legacy specific oxide-modification technique involves introducing boron into the oxide layer.[11] This suppresses the trapped charge and stabilizes the transistor switching voltage under ionizing radiation.

RHBD is a well-established technology to protect electronic equipment from radiation. Microchip's Radiation-Tolerant Generation 4 (RTG4) field-programmable gate array (FPGA) is an example of this and is radiation-hardened against single-event upsets.[12] RTG4 FPGAs were flown on the CAS500-1 Earth observation satellite launched into LEO in 2021 by the Republic of Korea.[13]

However, RHBD methods add cost to conventional transistors because their geometries occupy chip area otherwise used for computing and require dedicated fabrication processes, which makes doped transistors challenging to scale commercially. This also means that SBDCs would not be able to use commodity AI processors.

iii. Redundancy

Triple modular redundancy allows for critical functions to run on three separate processors at once and uses a voting circuit to accept the result at least two of the three agree on.[14] This redundancy protects against a potential single corrupted result from an SEE from a high-energy particle strike.

This is a well-established technology already used on National Aeronautics and Space Administration (NASA)-crewed missions, such as Artemis II, on which Orion stores data in triplicate and performs a best-of-three vote on every read to correct single-bit errors.[15] Yet, tripling the number of processors triples the mass and energy consumption of affected equipment, dramatically increasing the cost of AI hardware in space.

iv. Specialized materials

Chips can be built silicon-on-insulator, where an insulating oxide layer also sits beneath the silicon to limit the charge generated by a particle strike or cumulative damage.[16] Implanting ions, such as fluorine, into the lower oxide layer during fabrication can increase the cumulative radiation dose a chip can tolerate.[17]

This is a well-established process. Honeywell manufactures radiation-hardened processors, such as the HX1750 with its silicon-on-insulator method, specifically for spacecraft applications.[18] While the manufacturing process is mature, extending it to modern AI chips will incur process engineering costs and would mean that SBDCs could not use commodity AI chips.

v. Software-based hardening

Software can be used to monitor high-radiation conditions and intentionally reduce electronic equipment's power and processing speed during these periods to reduce the chance of SEEs. This was tested by Hewlett Packard Enterprise (HPE) on an unmodified commercial supercomputer on the International Space Station (ISS) starting in 2017 (see Figure 9); the computer ran successfully for 1.5 years.[19]

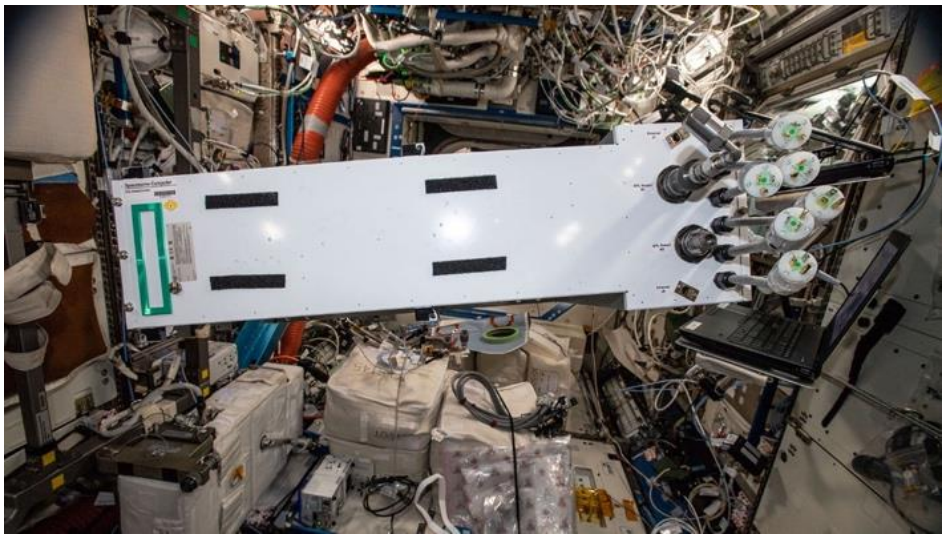


Figure 9. Hewlett Packard Enterprise's Spaceborne Computer-1 on the ISS. Source: NASA

This method, however, does not reduce TID and overall reduces the amount of compute each satellite can deliver, raising costs and decreasing efficiency. Moreover, this technology has only been tested in orbit at small scale, and the HPE system's software responded to general conditions outside established parameters rather than mitigating radiation specifically. This approach is therefore not yet established at the scale or specificity that a dedicated set of AI chips in LEO would require.

vi. Software tolerance

This method assumes errors in some parts of a software model are more sensitive than in others and redesigns the model to absorb these errors in the most sensitive layers. It was tested on a satellite-image classification model using hardware identical to that on China's Chaohu-1 satellite, and the method reduced the model's crash rate from 96% to 0% under equivalent radiation-error conditions.[20]

This approach, however, requires modification and retraining of models specific to their architectures, incurring additional engineering effort and cost. While this technology was validated in a ground test, it will require substantial further investment to be operationally established in LEO. However, one important advantage of this approach is that it could be deployed on satellites that are already in orbit via software updates, allowing it to immediately provide benefits (see Text Box 1-2 Software).

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